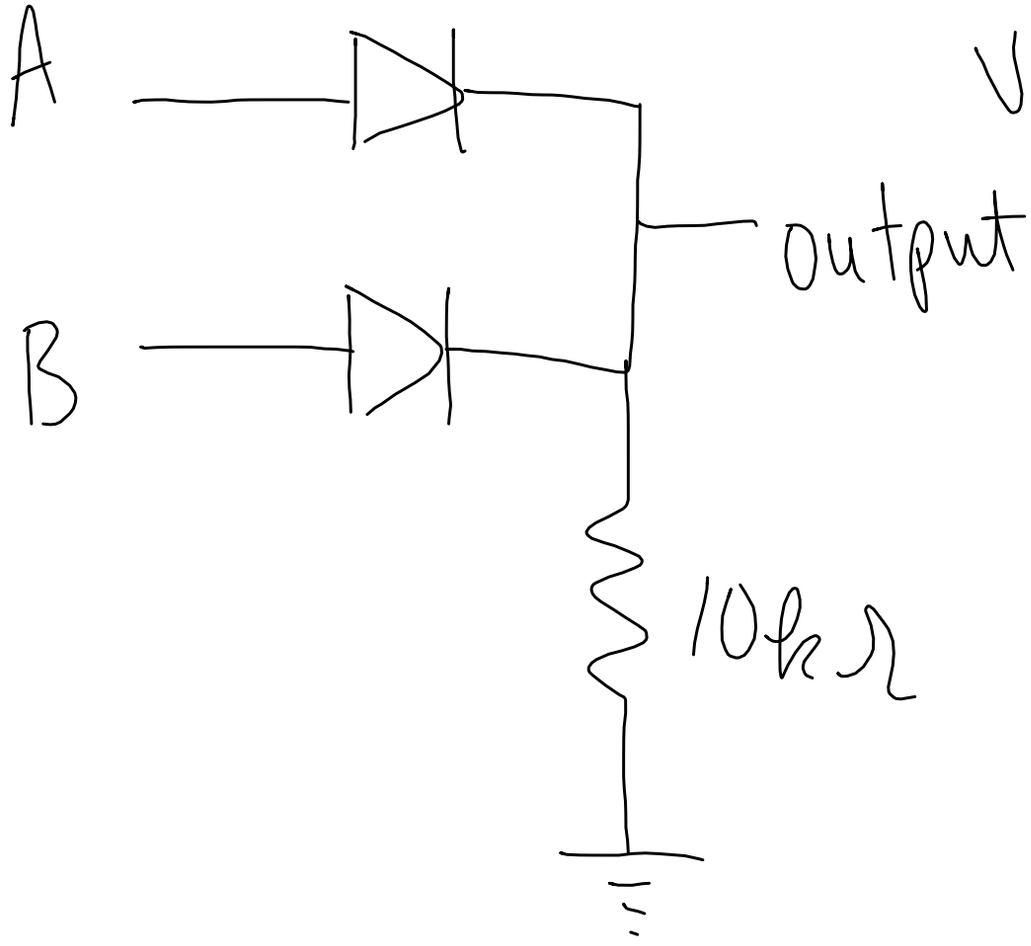
Diode logic

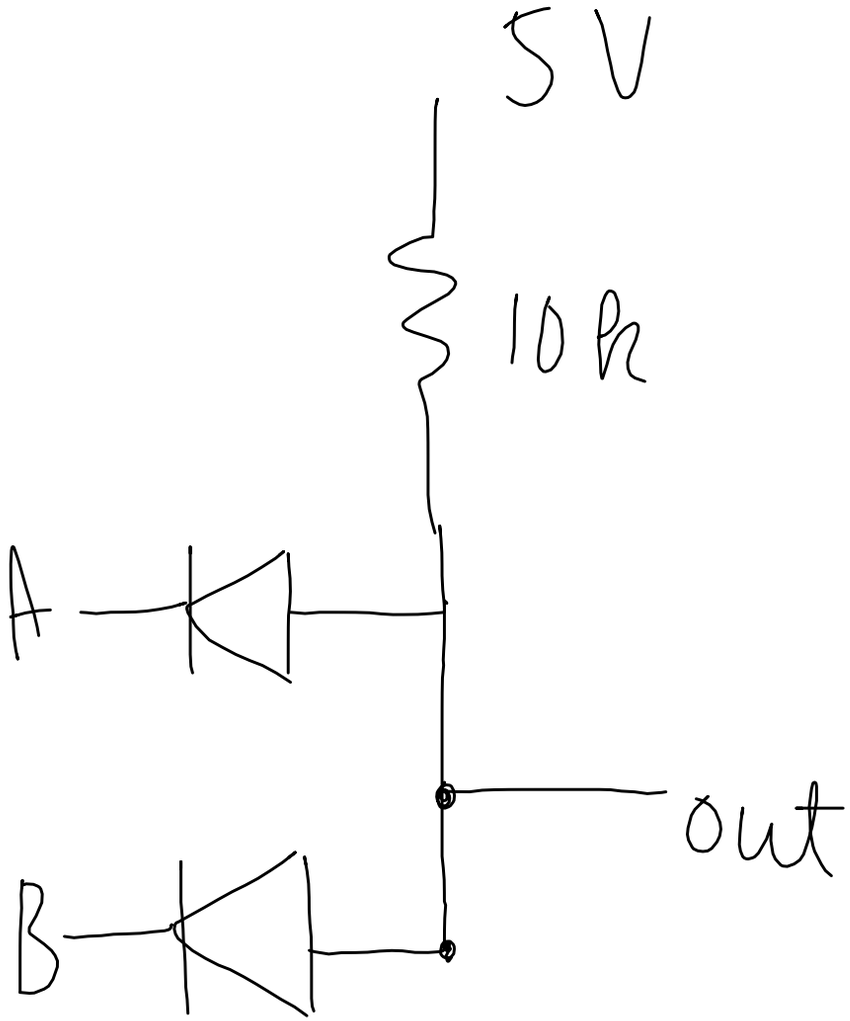
A & B are logic voltages (0 or 5 V)



A	B	Out
0	0	0
5	0	≈5
0	5	≈5
5	5	≈5

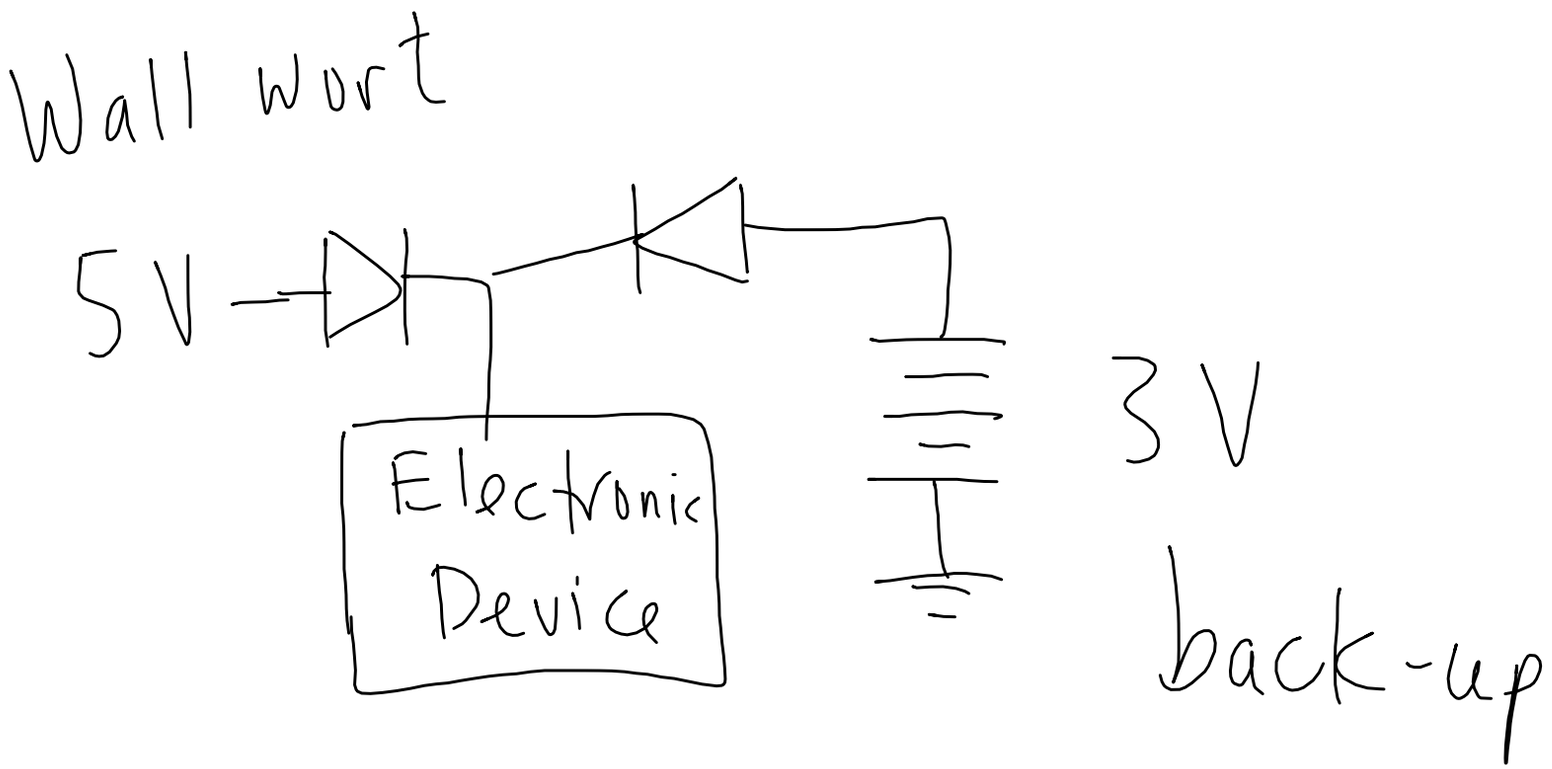
A	B	out
F	F	F
T	F	T
F	T	T
T	T	T

"OR"

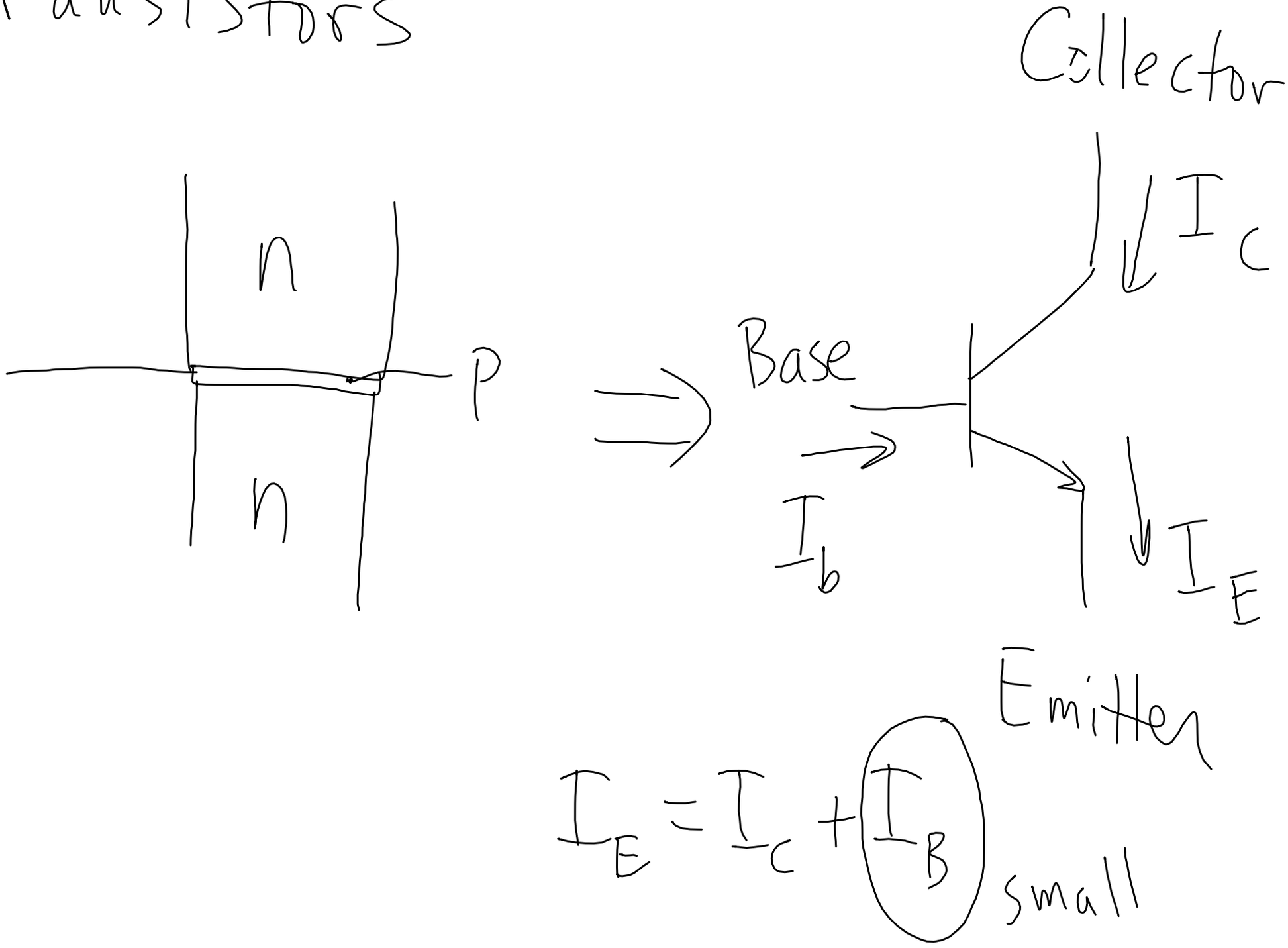


A	B	out
0	0	0
0	1	0
1	0	0
1	1	1

"AND"


Wall wart
5V
Electronic Device
3V
back-up

Transistors



$$I_E = I_C + I_B$$

small

$$I_C = \beta I_B$$

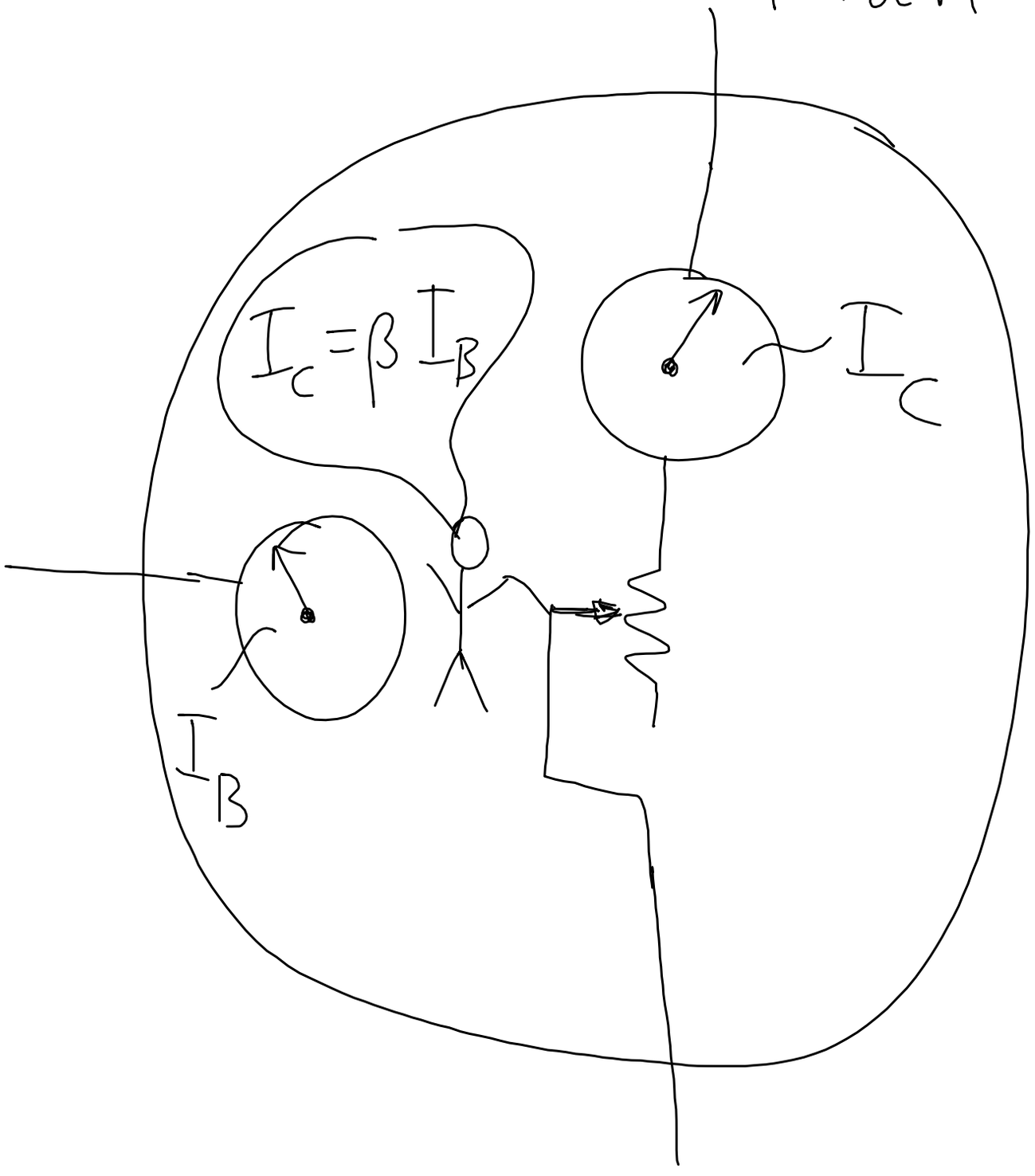
β or h_{FE}

current gain of transistor

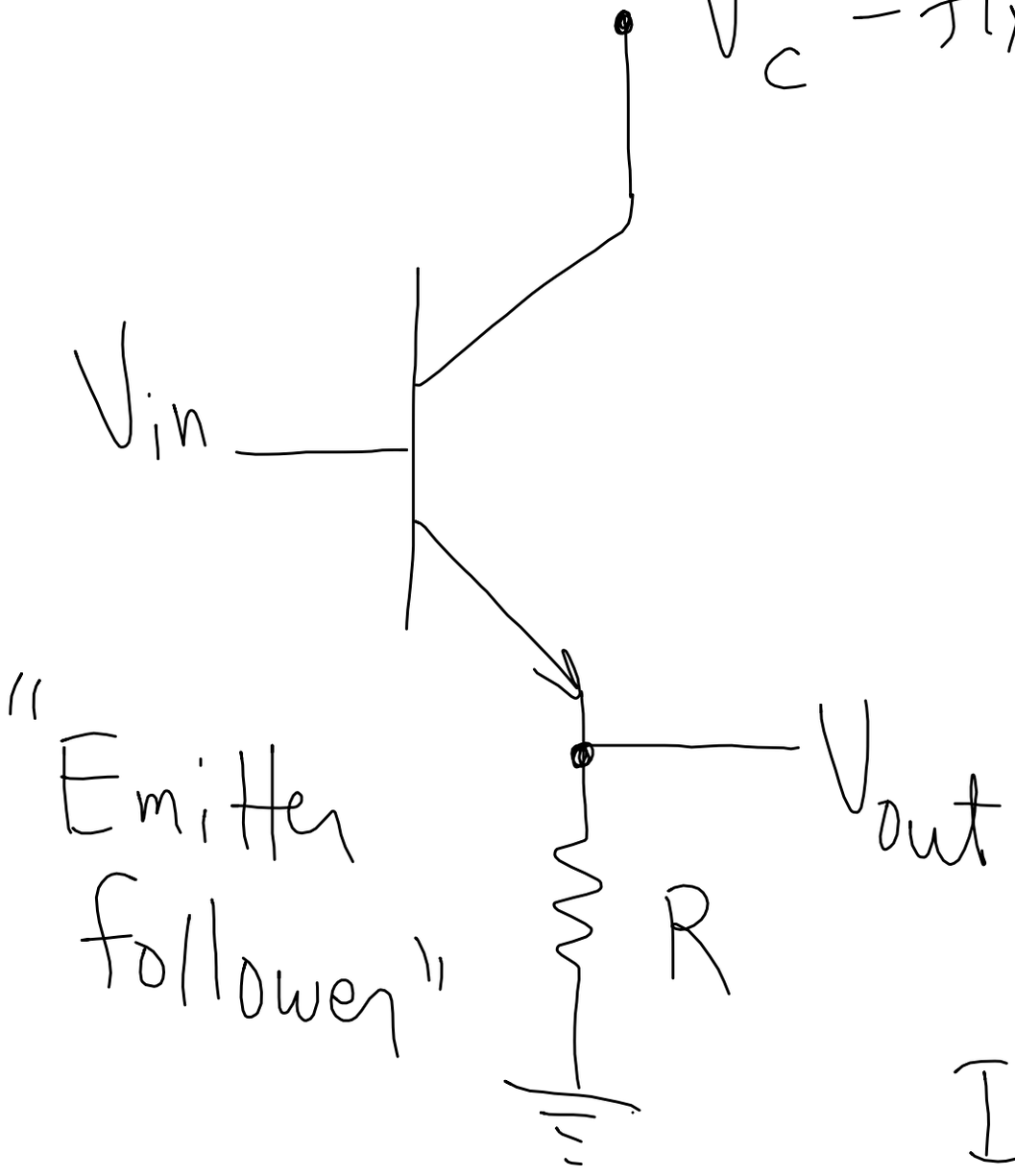
$\beta \approx 10 - 400$

β is not good design parameter

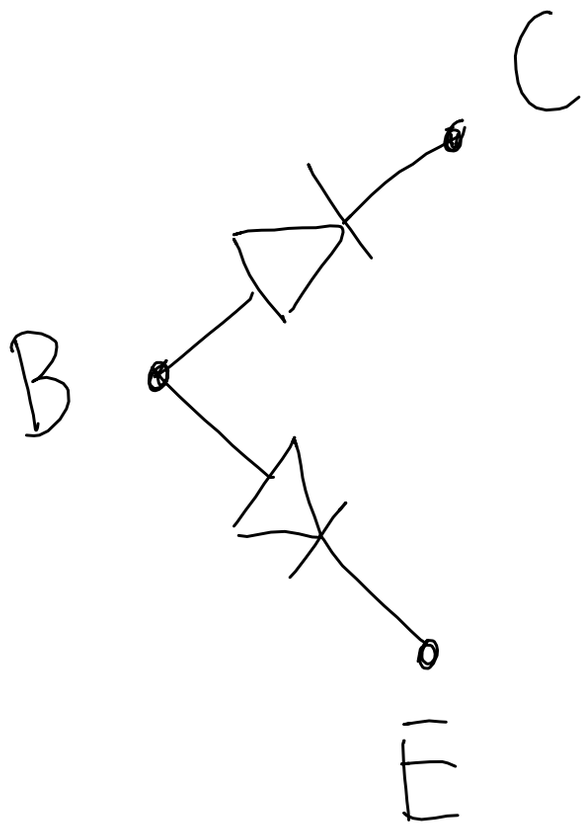
Transistor Man



V_c = fixed power supply



"Emitter follower"



use this picture

If $V_{in} = 5V$, $V_{out} \doteq 4.3V$

Rules: (for npn)

1. $V_{CE} > 0$

2. BE + BC act like diodes

3. Max values can't be exceeded

4. $I_C = \beta I_B$

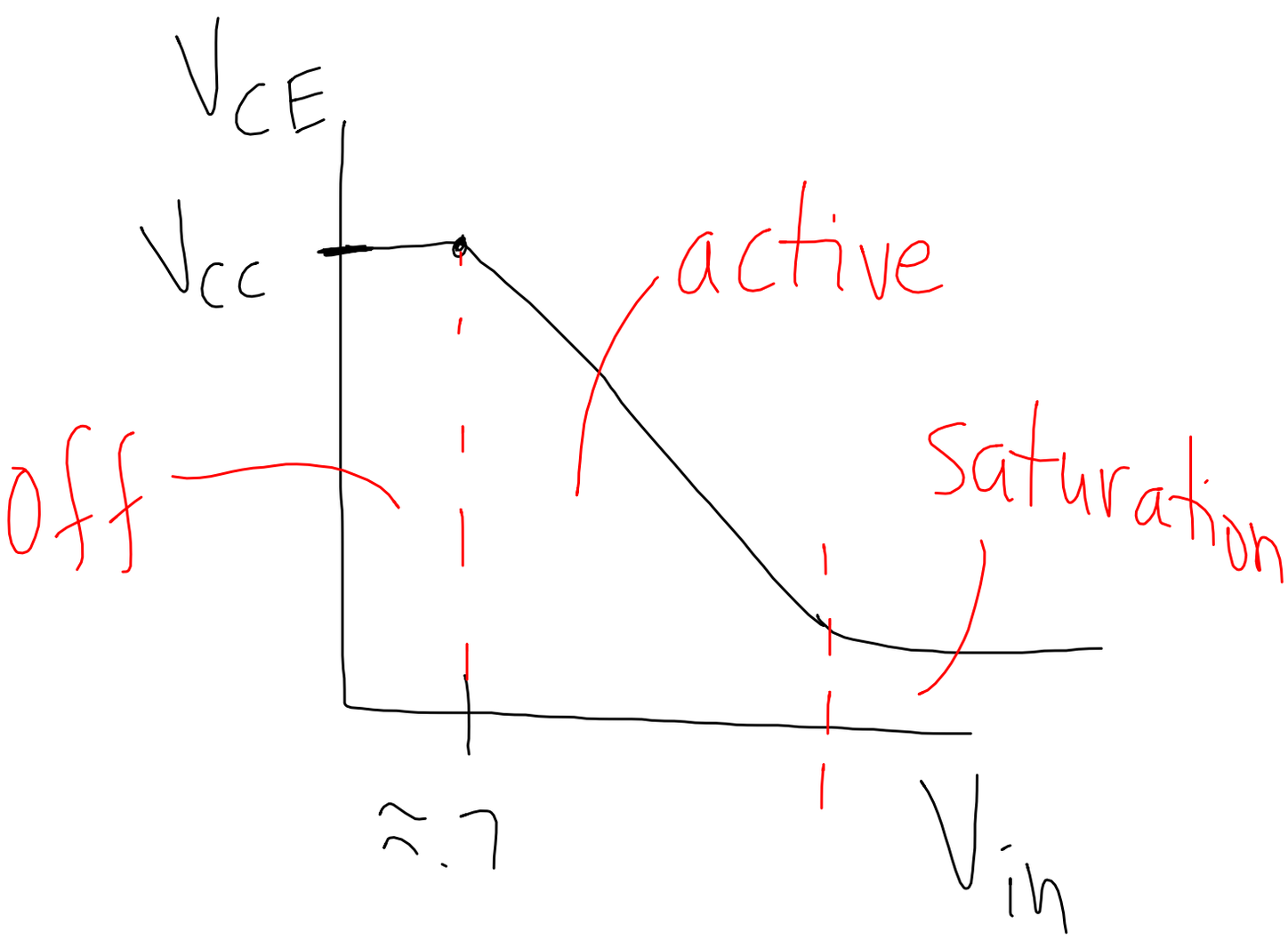
Since β is not very constant,

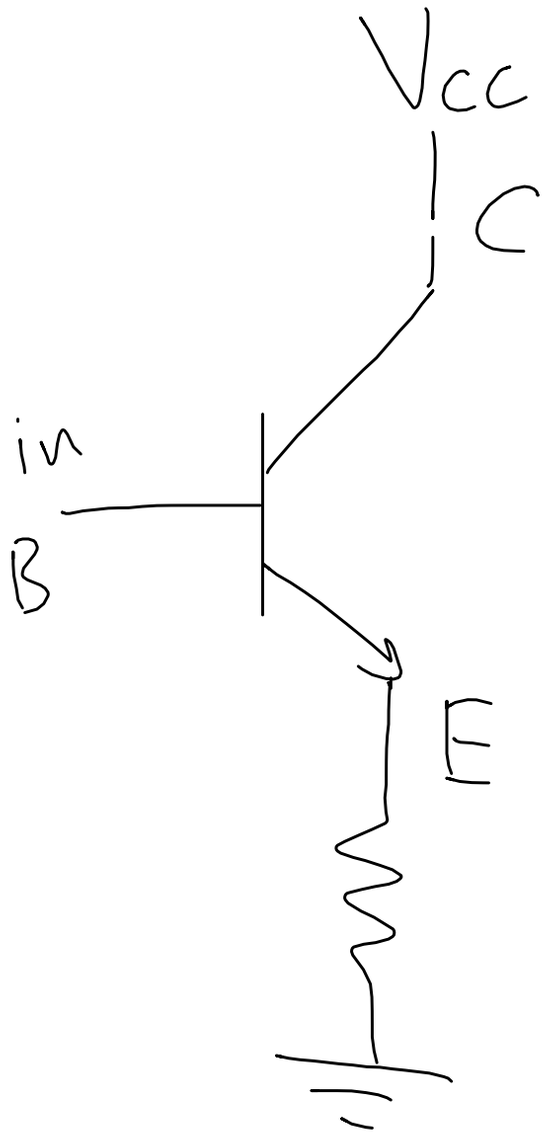
Replace rule # 4 with

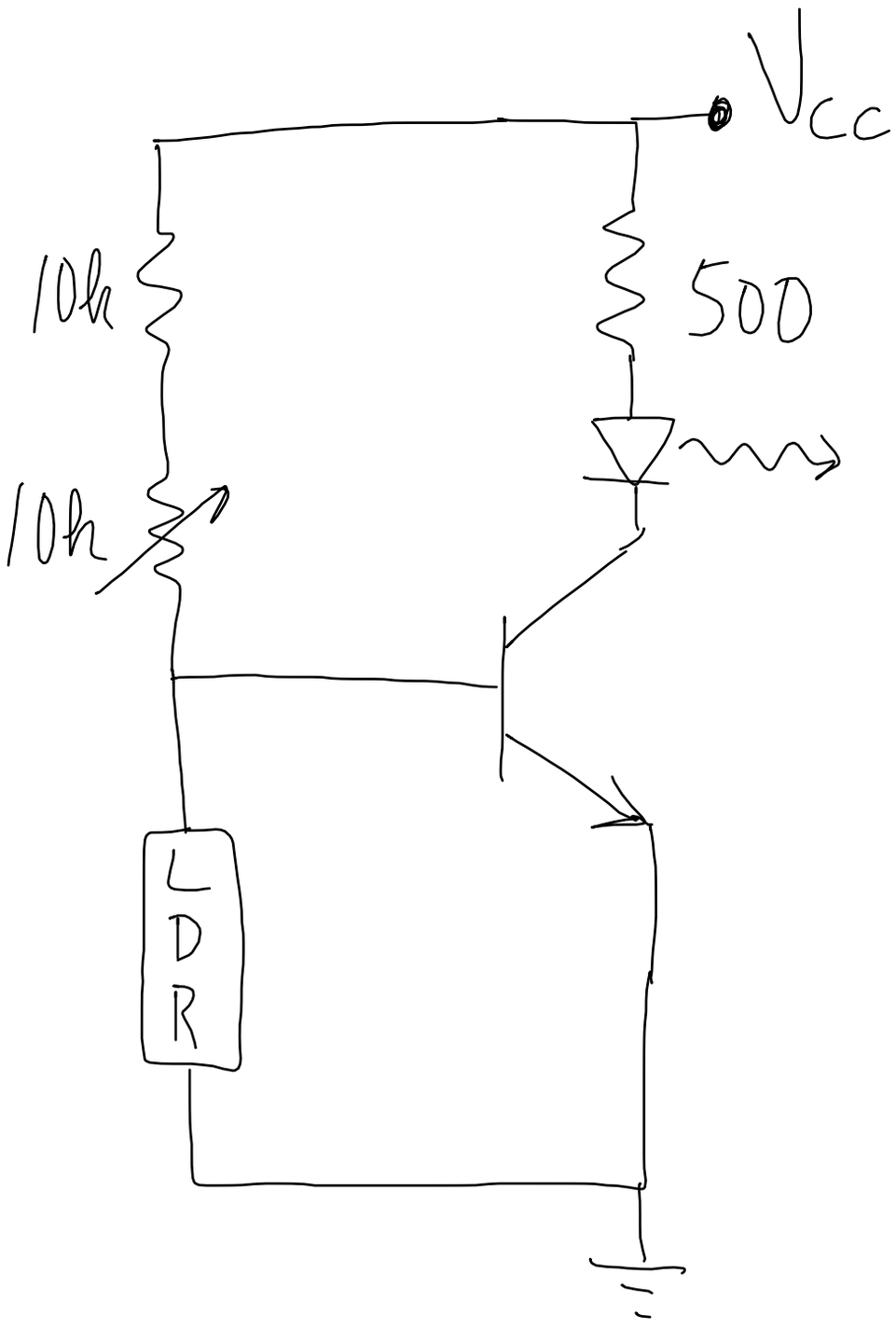
$$I_C = I_{sat}\left(e^{V_{BE}/V_T} - 1\right)$$

$$V_T = \frac{k_B T}{e}$$

Ebers-Moll model


V_{CE}
V_{CC}
active
off
saturation
$\approx .7$
V_{in}


V_{CC}
C
in
B
E



Assume R_{LDR} increases as light hits it.